

IN THE CLAIMS

Please amend the claims as follows.

1. (Previously Presented) A ball grid array device comprising:
a substrate, further including:
 a first major surface; and
 a second major surface; and
an array of pads made of an electrically conductive material, the array of pads positioned on the first major surface; and
a solder ball formed on at least one of the array of pads, at least one of the array of pads including a solderable diffusion retarding layer for controlling the out-diffusion of the electrically conductive material from the at least one pad during a solder reflow process.
2. (Original) The ball grid array device of claim 1 further comprising a binding layer for binding the diffusion retarding layer to the conductive material of the at least one pad.
3. (Original) The ball grid array device of claim 2 further comprising a layer of material for receiving solder.
4. (Original) The ball grid array device of claim 2 further comprising a layer of material for receiving solder placed on the diffusion retarding layer.
5. (Original) The ball grid array device of claim 1 wherein the electrically conductive of the pad includes copper.
6. (Original) The ball grid array device of claim 1 wherein the diffusion retarding layer includes Kovar®.

7. (Original) The ball grid array device of claim 1 wherein the diffusion retarding layer includes 54Fe-29Ni-17Co.

8. (Original) The ball grid array device of claim 2 wherein the binding layer includes Titanium (Ti).

9. (Original) The ball grid array device of claim 2 wherein the binding layer is Titanium (Ti).

10. (Original) The ball grid array device of claim 9 wherein the Titanium binding layer has a thickness in the range of 80 nanometers (nm) to 120 nanometers (nm).

11. (Original) The ball grid array device of claim 9 wherein the Titanium binding layer has a thickness in the range of 90 nanometers (nm) to 110 nanometers (nm).

12. (Original) The ball grid array device of claim 4 wherein the layer of material for receiving solder includes gold (Au).

13. (Original) The ball grid array device of claim 4 wherein the layer of material for receiving solder is gold (Au).

14. (Original) A substrate comprising:
at least one pad of a copper material;
a diffusion retarding layer placed over the at least one pad; and
a layer of gold over the at least one pad diffusion retarding layer.

15. (Original) The substrate of claim 14 wherein the diffusion retarding layer includes 54Fe-29Ni-17Co.

16. (Original) The substrate of claim 14 further comprising a layer of titanium (Ti) used to bond the diffusion retarding layer to the material of the at least one pad.

17. (Original) The substrate of claim 14 wherein the diffusion retarding layer includes 54Fe-29Ni-17Co, the substrate further comprising a layer of titanium (Ti) used to bond the diffusion retarding layer to the material of the at least one pad.

18. (Original) The substrate of claim 14 further comprising a plurality of pads.

19. (Original) The substrate of claim 14 further comprising a plurality of pads arranged in an array.

20. - 27. (Canceled)

28. (Previously Presented) A ball grid array device comprising:
a substrate including a first major surface, the substrate further including an array of pads made of an electrically conductive material, the array of pads positioned on the first major surface;
a diffusion retarding layer placed on at least one of the array of pads; and
solder placed on at least one of the array of pads, the solder and the pad including a intermetallic compound including Ni-Sn (Ni_3Sn_4) and Sn-Fe.

29. (Original) The ball grid array device of claim 28 wherein the solder is lead-free.

30. (Original) The ball grid array device of claim 28 wherein the pad includes a layer of gold.

31. (Previously Presented) An electronic device comprising:
a copper pad on the electronic device; and

means to retard diffusion of the copper associated with the copper pad adapted to retard the out-diffusion of the copper from the pad during a solder reflow process.

32. (Previously Presented) The electronic device of claim 31 wherein the means to retard diffusion of the copper includes a layer of binding material.

33. (Previously Presented) The electronic device of claim 31 further comprising a layer of solderability enhancing material attached to the means to retard diffusion.

34. (Previously Presented) The electronic device of claim 31 further comprising means for binding the pad and the means to retard diffusion; and a solderable layer of material attached to the copper pad.

35. (Previously Presented) A ball grid array device comprising:
a substrate;
a copper pad on the substrate;
means to retard diffusion of the copper associated with the copper pad; and
a solder ball attached to the copper pad .

36. (Previously Presented) The ball grid array device of claim 35 wherein the solder ball is formed from a lead free material.

37. (Previously Presented) The ball grid array device of claim 35 further comprising a binder for attaching the means to retard copper to the copper pad.

38. (Previously Presented) The ball grid array device of claim 37 wherein the binder includes a layer of titanium (Ti) on the copper pad.

39. (Previously Presented) The ball grid array device of claim 35 further comprising a layer of gold associated with the means to retard diffusion of copper.

AMENDMENT UNDER 37 C.F.R. 1.116 – EXPEDITED PROCEDURE

Serial Number: 10/673,605

Filing Date: September 29, 2003

Title: DIFFUSION BARRIER LAYER FOR LEAD FREE PACKAGE SUBSTRATE

Assignee: Intel Corporation

Page 7

Dkt: 884.A68US1 (INTEL)

40. (Canceled)